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Methods of designing analog-to-digital converters design trend review

An increase of demand for high-speed communications leads to increasing the requirements for the interface between the digital and analog domains. That is why now design of high-performance analog-to-digital (ADC) and digital-to-analog (DAC) converters becomes so important. A lot of publications are dedicated to enhancement of ADC and DAC performance.

For a CMOS ADC with sampling rates above 10GHz, the timeinterleaved architecture is an effective approach exploiting the superior performance of CMOS switched-capacitor circuits [1]. Technology scaling allows designing higher rate converters using an interleaved architecture of SAR ADCs. Recently, 40Gb/s CMOS ADCs were reported based on an interleaved SAR architecture [2].

For increasing the linearity even traditional Nyquist-rate converters such as pipeline and SAR ADCs are operated with oversampling ratio greater than 1 (OSR>1). This allows the use of dynamic element matching (DEM) technic [3]. DEM is a dynamic process that reduces the effects of component mismatches in electronic circuits by rearranging dynamically the interconnections of mismatched components so that the time averages of the equivalent components at each of the component positions are equal or nearly equal [4].

A very effective technic to cope with noise, as well as other error sources (capacitor mismatch, finite sampling bandwidth, comparator hysteresis), is concept of a SAR ADC with redundancy [3]. Converters with redundancy use codes with bases smaller than 2 (not binary). There are several digital codes for every input voltage, so small errors do not affect the conversion result.

For low power consumption Charge-Redistribution ADCs are used. Only the comparator and the dynamic charging and discharging of the capacitive array determine the power consumption of the scheme. For some further power reduction the capacitor arrays are not completely binary weighted, but use a split capacitor bank, thus power consumption of only 1.9mW can be achieved for 10b ADC [5].

Analysis and conclusions are based on more than 25 scientific and technical publications which were published between years 1975–2010.

References

1. Peter Schvan, Jerome Bach, Chris Falt, Philip Flemke, Yuriy Greshishchev, Naim Ben-Hamida, Daniel Pollex, John Sitch, Shing-Chi Wang, John Wolczanski, "A 24GS/s 6b ADC in 90nm CMOS", ISSCC Dig. Tech. Papers, pp. 544–545, Feb. 2008.
2. Yuriy M. Greshishchev, Jeorge Aguirre, Marinette Besson, Robert Gibbins, Chris Falt, Philip Flemke, Naim Ben-Hamida, Daniel Pollex, Peter Schvan, Shing-Chi Wang, "A 40GS/s 6b ADC in 65nm", ISSCC Dig. Tech. Papers, pp. 390–391, Feb. 2010.
3. M. Hesener, T. Eichler, A. Hanneberg, D. Herbiso, F. Kuttner, H. Wenske, "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13mm CMOS", ISSCC Dig. Tech. Papers, pp. 248–249, Feb. 2007.
4. K.B. Klaasen, "Digitally controlled absolute voltage division," IEEE Trans. Instrumentation and Measurement, vol. 24, no. 2, pp. 106–112, June 1975.
5. Michiel van Elzakker, Ed van Tuij, Paul Geraedts, Daniel Schinkel, Eric Klumperink, Bram Nauta, " A 1.9mW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC", ISSCC Dig. Tech. Papers, pp. 244–245, Feb. 2008.

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